WHAT IS CLAIMED IS:

1. A configurable and scaleable multi-bus platform for developing, testing and/or debugging prototype systems to be implemented in an integrated circuit, the platform comprising:

a backplane providing a plurality of busses;

a plurality of system bus cards each physically coupleable to the backplane, each of the system bus cards comprising:

a system bus which is electrically coupled to a corresponding one of the plurality of busses provided by the backplane when the system bus card is physically coupled to the backplane; and

a bus infrastructure device providing support logic for operating the system bus on the system bus card; and

a plurality of daughter cards each physically coupleable to one of the plurality of system bus cards and including at least one master or slave device, wherein when a particular daughter card is physically coupled to one of the plurality of system bus cards then at least one master or slave device of the particular daughter card is in electrical communication with the system bus of the system bus card.

2. The configurable and scaleable multi-bus platform of claim 1, wherein the platform further comprises a multi-master/multi-slave multi-bus-port card which is physically coupleable to the backplane, wherein the multi-master/multi-slave multi-bus-port card includes at least one interface device, and wherein when the multi-master/multi-slave multi-bus-port card is physically coupled to the backplane then at least one interface device is in electrical communication with one or more of the busses provided by the backplane.

3. The configurable and scaleable multi-bus platform of claim 1, wherein the bus infrastructure device of each of the plurality of system bus cards further comprises a bus arbiter.

4. The configurable and scaleable multi-bus platform of claim 3, wherein the bus infrastructure device of each of the plurality of system bus cards further comprises an address decoder.

5. The configurable and scaleable multi-bus platform of claim 4, wherein the system bus of each of the plurality of system bus cards further comprises a multi-master bus and a multi-slave bus, and wherein when daughter cards are physically coupled to a particular system bus card, master and slave devices on the daughter cards are electrically

coupled to the multi-master bus and the multi-slave bus, respectively.

6. The configurable and scaleable multi-bus platform of claim 5, wherein the plurality of daughter cards includes master daughter cards having master devices thereon, and slave daughter cards having slave devices thereon.

7. The configurable and scaleable multi-bus platform of claim 6, wherein each system bus card further comprises a statistic generating device coupled to the system bus, the statistic generating device generating statistical information indicative of the performance of the system.

8. The configurable and scaleable multi-bus platform of claim 6, wherein each system bus card further comprises a debugging device which aids in debugging errors in the system.

9. The configurable and scaleable multi-bus platform of claim 6, wherein one or more of the plurality of daughter cards contain intellectual property devices to be integrated as masters/slaves in silicon.

10. The configurable and scaleable multi-bus platform of claim 7, wherein a daughter card containing an intellectual property device also includes a field programmable gate array configured

to interface between the intellectual property device and a system bus on the corresponding system bus card.

11. The configurable and scaleable multi-bus platform of claim 6, wherein one or more of the plurality of daughter cards contain central processing units.

12. The configurable and scaleable multi-bus platform of claim 6, wherein at least one of the plurality of daughter cards contains a graphics engine device.

13. A configurable and scaleable multi-bus platform for developing, testing and/or debugging prototype systems to be implemented in an integrated chip, the platform comprising:

a backplane providing a plurality of busses;

a plurality of substantially identical system bus cards each physically coupleable to the backplane, each of the system bus cards comprising:

a system bus which is electrically coupled to at least one of the plurality of busses provided by the backplane when the system bus card is physically coupled to the backplane; and

a bus infrastructure device providing support logic for operating the system bus on the system bus card; and

a plurality of daughter cards each physically coupleable to one of the plurality of system bus cards and including at least one master or slave device, wherein when a particular daughter card is physically coupled to one of the plurality of system bus cards then at least one master or slave device of the particular daughter card is in electrical communication with the system bus of the system bus card.

14. The configurable and scaleable multi-bus platform of claim 13, wherein for each of the plurality of system bus cards, the corresponding daughter cards coupled to that system bus card function with the system bus card to model a corresponding system bus on an integrated circuit to be implemented.

15. The configurable and scaleable multi-bus platform of claim 14, wherein the platform further comprises a multi-master/multi-slave multi-bus-port card which is physically coupleable to the backplane, wherein the multi-master/multi-slave multi-bus-port card includes at least one interface device, and wherein when the multi-master/multi-slave multi-bus-

port card is physically coupled to the backplane then at least one interface device is in electrical communication with one or more of the busses provided by the backplane.

16. The configurable and scaleable multi-bus platform of claim 13, wherein the bus infrastructure device of each of the plurality of system bus cards further comprises a bus arbiter and an address decoder.

17. A configurable and scaleable multi-bus platform for developing, testing and/or debugging prototype systems to be implemented in an integrated chip, the platform comprising:

backplane means for providing a plurality of busses;

bus card means coupled to the backplane means for providing a plurality of system busses coupled to the plurality of busses provided by the backplane means; and

daughter card means for configuring the bus card means in order to model a corresponding system bus on an integrated circuit to be implemented.